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PROPERTIES OF DEVICES PREPARED WITH EPITAXIAL LAYERS ON InP

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Electrical measurements were made on capacitors prepared with RPECVD SiO_2 films on p-type $Ga_{0.47}In_{0.53}As$ at low substrate temperatures. These measurements demonstrated that the RPECVD dielectric is suitable for use in the fabrication of MISFETs. Measurements on RPECVD SiO_2 layers on Si showed that care must be taken in cleaning and processing to prevent Na ions from being introduced into the dielectric layers. To provide stable characteristics, surface cleaning before deposition must be investigated and processing techniques must be used to prevent the introduction of mobile ions into the deposited dielectric layers. Techniques to reduce the temperature sensitivity of the threshold current density of InP-$Ga_xIn_{1-y}As_yP_{1-y}$ DH lasers were investigated. The most promising technique is the use of thin pseudomorphic active layers and wide energy gap cladding layers.

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Properties of Devices Prepared with Epitaxial Layers on InP

I. SUMMARY

The properties of devices prepared with epitaxial layers on InP were investigated. Both metal-insulator-semiconductor (MIS) structures and double heterostructure (DH) lasers were considered. The MIS structures were fabricated with a low temperature remote plasma-enhanced chemical-vapor deposition (RPECVD) of the insulating dielectric. Layers were evaluated by capacitance-voltage (C-V) measurements. Also, possible material systems which could reduce the leakage current in $Ga_xIn_{1-y}As_yP_{1-y}$ active layers due to Auger recombination were examined.

For investigation of RPECVD dielectric layers on $Ga_{0.47}In_{0.53}As$, variable frequency capacitance vs. gate voltage measurements were made on $Ga_{0.47}In_{0.53}As$ MIS capacitors prepared by the Research Triangle Institute (RTI). The insulating layers were deposited on p-type $Ga_{0.47}In_{0.53}As$ layers grown on conducting p-type InP substrates. Extensive C-V measurements demonstrated that the dielectric layers which were deposited by RPECVD with a substrate temperature of 350°C have small hysteresis and can achieve inversion. These RPECVD insulating layers have the required properties for the development of a MISFET technology for $Ga_{0.47}In_{0.53}As$ layers grown on InP. The next step in the development of this technology is to determine the proper cleaning

procedures before insulator deposition and the processing technology which prevents contamination with mobile ions such as Na. Numerous electrical and surface analytical instruments have been added to the laboratory to permit a detailed investigation of the InP and $Ga_{0.47}In_{0.53}As$ interface with the RPECVD SiO_2. These tools will be used for the development of reliable and reproducible techniques in the preparation of stable and drift free MISFET devices with InP and $Ga_{0.47}In_{0.53}As$.

To provide larger conduction and valence band discontinuities at the active and cladding layer interfaces of $Ga_xIn_{1-y}As_yP_{1-y}$ DH lasers, strained layer and pseudomorphic layers were considered. A larger conduction and valence band discontinuity than at the InP - $Ga_xIn_{1-y}As_yP_{1-y}$ interface would confine the energetic carriers which result because of Auger recombination and cause excessive leakage current. The most promising approach appears to a pseudomorphic active layer. For a pseudomorphic active layer, a critical thickness exists at which layers of less thickness can be grown without lattice match and still remain free of mismatch dislocations. Single quantum well lasers with active layer thicknesses up to 100 $\mathring{A}$ could have wide energy gap cladding layers which can confine the hot carriers which result from Auger recombination in the active layer.

II. $Ga_{0.47}In_{0.53}As$-InP MIS DEVICES

A. MIS Measurements

Metal-insulator-semiconductor capacitors were prepared by RTI by remote plasma enhanced chemical vapor deposition.[1] The p-type

$Ga_{0.47}In_{0.53}As$ layer was grown on a p-type InP substrate by liquid-phase epitaxy (LPE). Special care was taken in the deposition of the plasma oxide in order to minimize native oxide growth. In the RTI process, the metastable oxygen species formed in the plasma react with monosilane to produce disilane. A composite insulator structure was used to minimize native oxide growth. A thin silicon dioxide layer is used on the semiconductor surface to control the interface density, then a thicker silicon nitride layer serves as a diffusion barrier to oxygen. The total dielectric thickness is typically near 450 Å.

The variable frequency capacitance-voltage (C-V) and conductance-voltage (G-V) measurements of the MIS capacitors were made with a lock-in voltmeter. When the phase angle of the lock-in voltmeter is set at 0^{o}, G-V measurements can be made, while the phase is set at 90^{o} to measure the C-V behavior. The current flowing through the capacitor is converted to voltage by a current-to-voltage converter that uses a large input impedance op-amp. The output of the op-amp is connected to the lock-in voltmeter and the 0^{o} or 90^{o} current component is selected. Measured data is transferred to the HP-4145 semiconductor parameter analyzer and to the HP-9000-217 computer. These data are stored for further analysis and can be plotted on the x-y plotter.

The C-V behavior from 500 Hz to 1 MHz is summarized in Figs. 1-6. The gate voltage variation was limited between -5 V and +5 V to prevent damage to the dielectric. Accumulation is approached at -5 V and inversion is achieved for voltages in excess of +1 V. As the measurement frequency exceeds 50 kHZ, the thermal generation time becomes too long

to achieve inversion for such a high frequency. The conductance at 10 kHz and 1 MHz is shown in Figs. 7 and 8, respectively. The conductance measurements show that the problems with series resistance which were encountered with p-$Ga_{0.47}In_{0.53}As$ on semi-insulating InP are no longer present.

The temperature stress bias measurement[2] and the triangular voltage sweep measurement[3] indicated the presence of mobile ions in the dielectric layers. In order to simply the analysis, a better known Si MIS capacitor was used for evaluation instead of the $Ga_{0.47}In_{0.53}As$ MIS capacitor. The Si MIS capacitor has a 1000 Å RPECVD SiO_2 film deposited on a p-type Si substrate which is doped to $1x10^{15}$ cm^{-3}. As a metal electrode, Al with an area of $2.5x10^{-3}$ cm^2 was deposited on top of the SiO_2. This Si MIS capacitor was prepared at RTI for research on plasma deposited dielectrics in conjunction with North Carolina State University under ONR contracts (Contract No. N00014-79-C-0133 and N00014-84-C-0659) and under a NAVELEX contract Contract No. N00039-81-C-0661). The capacitor was made available to us for further characterization.

The 1 MHz C-V measurement is shown in Fig. 9. The solid curve was swept from -8 to 12 V, and the dotted curve was swept from 12 to -8 V. The gentle descent from accumulation to the depletion region indicates the existence of surface states at the SiO_2-Si interface, and the hysteresis in the curve indicates a slow charge distribution in the oxide.

The amount of Na ions in the SiO_2 film was measured by both temperature stress bias measurement and triangular voltage sweep (TVS) measurement. The temperature stress bias measurement is done by

measuring the 1 MHz C-V curve at room temperature. Then the capacitor is heated to 250°C for 5 min. This time ensures that all the available mobile ions will drift completely across the oxide. The capacitor is cooled down to room temperature with the bias on the metal. The positive bias will drift the positively charged mobile ions toward the SiO_2-Si interface, which results in a shift in the 1 MHz C-V curve when measured again at room temperature. The measured results with biases of +5 V and +10 V are shown in Figs. 10 and 11. The measurement with a bias of +5 V showed that the curve shifted toward lower bias, which is expected due to redistribution of mobile ions. However, with a bias of +10 V, the curve shifted toward higher bias. These results suggest that the temperature stress bias measurement alters not only the mobile ion distribution in the SiO_2 film, but some other properties that will affect the flat band voltage of the RPECVD SiO_2-Si MIS capacitor.

The TVS measurement was performed in a high temperature ambient where the Na ions in the SiO_2 film are mobile. A voltage sweep is applied between the metal and the semiconductor, and the current flowing through the capacitor is measured with a Keithley 642 electrometer. This voltage is swept very slowly (less than 50 mV/sec) from negative to positive bias, and back to negative bias. The measured result is shown in Fig. 12. Two peaks in the current indicate the ion drift inside the SiO_2 film. The number of drifted mobile ions is calculated to be approximately 1.3×10^{13} cm^{-2}. However, this result does not show a difference in Na ion mobilities for drift from the metal-SiO_2 interface to the Si-SiO_2 interface direction and the opposite direction, which is typically seen in thermally

grown SiO_2 films.[4] The TVS measurement performed on thermally grown SiO_2-Si MIS capacitors usually exhibits a large peak in current when the bias is swept from positive to negative. This difference is due to the difference in potential well depths at the metal-SiO_2 interfaces. Thus, it can not be concluded that the current measured in this TVS measurement is the result of the Na ion drift in the SiO_2 film.

The existence of Na ions in the RPECVD SiO_2 was confirmed by the thermally stimulated ionic current (TSIC) measurement.[5] This measurement is similar to the TVS measurement. In this measurement, the temperature is ramped from -30°C to 240°C, and the bias voltage is maintained constant. The temperature of the wafer was altered with liquid nitrogen for cooling and a resistance heater for above room temperature. The measured result is shown in Fig. 13. This result indicates that all the ions in the SiO_2 film become mobile at a temperature near 0°C. Previous studies had shown that the Na ions begin to become mobile near 0°C; however, other commonly found mobile ions in SiO_2 such as K ions do not become mobile until the temperature reaches approximately 200°C.[5] Therefore, this measured result clearly indicates that the ion drift seen in the TVS measurement is due to Na ions. The TVS measurement also shows that the mobility of the Na ions are almost the same in both the metal-SiO_2 interface to the SiO_2-semiconductor interface direction or vice versa. This characteristic is not observed in the thermally grown oxide.

To reduce the Na contamination, a unique in-situ Si surface treatment was used. This surface treatment was evaluated in-situ with reflection high-energy electron diffraction (RHEED). The RHEED pattern for this

unique Si treatment indicated reconstruction of the Si surface, and MIS capacitors grown on these reconstructed Si surfaces exhibited characteristics comparable to thermally grown SiO_2 with very low interface state density and very low Na contamination. The SiO_2-Si work was a collaborative effort between RTI and North Carolina State University and demonstrated that the RPECVD was capable of producing high quality SiO_2 layers.

With the knowledge that the RPECVD was capable of producing high quality insulating layers, an investigation was undertaken to determine the optimum surface treatment prior to deposition of the RPECVD SiO_2 on InP. These surface treatments were evaluated by photoluminescence (PL) measurements. The observed PL is the light emitted when the photo-excited electron-hole pairs recombine radiatively.[6] The samples were excited with an argon laser, and the non-radiative surface recombination competes with the radiative bulk recombination. Therefore, the emission intensity is sensitive to the surface recombination. The PL measurements were made at 77K. For the Br based etches, the PL intensities are approximately 300 times greater than for the untreated InP. A variety of other etches did not change the PL intensity from the untreated InP.

B. New Electrical and Surface Analysis Equipment

A C-V and G-V measurement system was built for fast and accurate data analysis. The system is capable of performing C-V and G-V measurements for small signal frequencies from 500 Hz–12 MHz, and quasi-static measurements. This system also permits thermal stress bias[2] and triangular sweep measurements[3] for measuring the mobile ion

concentration. The stage temperature can be varied from room temperature to 300°C. Two 200 W heaters raise the stage temperature to 300°C in 4 min. The stage can be cooled down to room temperature in about 4 min. with water running through the Cu tubing. The temperature of the stage is measured with an iron-constantan thermocouple which is connected to a digital thermometer. The stage is electrically isolated and contained in a light tight Al box. Moisture on the sample is minimized by blowing dry nitrogen gas on the sample. A Micromanipulator model 44 probe is used to assure low parasitic capacitance and low noise.

Figure 14 illustrates the system configuration for quasi-static and TVS measurements. The small current flowing through the sample is measured by a Keithley model 602 electrometer while the HP-3314A function generator is used to generate a slow voltage ramp (less than 50 mV/sec). Figure 15 shows the system configuration for high frequency (1 MHz) C-V and G-V measurements and thermal stress bias measurements. Low to medium frequency (500 Hz to 1 kHz) C-V and G-V measurements are obtained by use of the lock-in amplifier as shown in Fig. 16. The PAR model 410 C-V plotter is controlled by the HP-9816 computer via a HP-6942A multiprogrammer which generates digital signals to control the plotter.

The data acquisition and analysis system is shown in Fig. 17. Measured signals are converted into digital signals by two analog-to-digital (A/D) converters which are installed in the HP-6942A multiprogrammer, and the HP-9816 computer acquires these digital signals. The acquired data are plotted either on the CRT screen of the computer or on the HP-

7475A plotter. Also, data can be stored on a disc for further analysis. Software for calculation of the C-V and G-V curves with corrections for series resistance, the interface state density from the high frequency C-V and quasi-static curves, and the mobile ion density from the thermal stress bias and TVS measurements are available.

Numerous analytical instruments, in addition to the existing ellipsometer at Duke, for surface analysis have been obtained by RTI and are available for studies of the InP and $Ga_{0.47}In_{0.53}As$ dielectric interface. The analytical tools now available for analysis of the RPECVD are: (a) ellipsometry for the measurement of the dielectric layer refractive index and thickness, (b) low energy electron diffraction (LEED), reflection high energy electron diffraction (RHEED), and ion scattering mass spectroscopy (ISS) for surface structure and absorbates determination, (c) Auger electron spectroscopy (AES) and angle resolved x-ray photoelectron spectroscopy (XPS) for determination of surface composition, depth profile and surface film thickness, (d) ultraviolet photoelectron spectroscopy (UPS) and energy loss spectroscopy (ELS) of the surface energy band structure. These tools are intended for detailed measurement of the InP and $Ga_{0.47}In_{0.53}As$ interface with the RPECVD SiO_2 to permit the development of reliable and reproducible techniques for the preparation of stable and drift free MISFET devices with InP and $Ga_{0.47}In_{0.53}As$.

III. InP-$Ga_xIn_{1-y}As_yP_{1-y}$ DOUBLE HETEROSTRUCTURE LASERS

A critical assessment of the threshold current density temperature

dependence for InP-$Ga_xIn_{1-y}As_yP_{1-y}$ double heterostructure lasers showed that the rapid increase in threshold current above room temperature was due to nonradiative Auger recombination and the leakage current which results due to the loss of the resulting hot carriers over the heterojunction barrier.[7] Two approaches were taken to determine what materials might be utilized to give a larger conduction and valence band discontinuity at the active and cladding layer interface. For a $Ga_xIn_{1-y}As_yP_{1-y}$ DH laser emitting at a wavelength of 1.3 μm, the energy gap would be 0.95 eV, while for an emission wavelength of 1.55 μm, the energy gap would be 0.80 eV. Therefore, to obtain an improved confinement of hot carriers to the active layer, an energy gap for the cladding layer would need to be in the range of approximately 1.5 to 2.0 eV.

In the case where an epitaxial layer does not have the same lattice constant as the substrate, the lattice mismatch can be accommodated either by elastic strain in the film or by misfit dislocations at the interface or by both. A very thin epitaxial film will be strained elastically to make its lattice constant equal to that of the substrate. As the thickness of the film increases, misfit dislocations that are formed at the interface begin to accommodate a larger and larger part of the mismatch. These dislocations are mainly edge dislocations. The transition for film being elastically strained to being full of dislocations is known to be quite abrupt.[8] Hence, a critical thickness, which is a function of lattice mismatch, can be defined for any epitaxial layer. It is the thickness at which the total strain energy (elastic and inelastic) is minimum. Also, the approximately inverse

relationship between the critical thickness of a film and lattice mismatch sets an upper limit on the lattice mismatch which is about 7 % for a monolayer. The critical thickness is given by[8]

$$h_c = \frac{b}{8\pi f} \frac{1 - \nu \cos^2 \alpha}{(1+\nu)\cos\lambda} \left[\ln\left(\frac{h_c}{b}\right) + 1\right],$$

where b is the bulk lattice constant, ν is Poisson's ratio (0.33), α is the angle between the Burger's vector and the dislocation line in the interface plane, h_c is the critical thickness of the layer, f is the misfit as a fraction, and λ is the angle between the Berger's vector and a line in the interface plane perpendicular to the line of intersection of the slip plane and the interface. For example, if a strained-layer superlattice (SLS) of InP and GaP is used as the cladding layer for a $Ga_xIn_{1-y}As_yP_{1-y}$ active layer, the maximum layer thickness for the GaP layer is about 15 Å because the misfit is quite large. Therefore, a ternary solid solution such a $Al_xIn_{1-x}As$ would permit thicker layers, but would be more difficult to grow.

A more promising approach would be to use a pseudomorphic active layer. For example, a plot of the critical thickness for a $Ga_xIn_{1-x}As$ layer on GaAs is shown in Fig. 18. The region below the curve results in a strained layer, while above the curve, the layer will have misfit dislocations. For an energy gap of 0.80 eV, x = 0.4 and the maximum layer thickness would be 20 Å. If $Al_xIn_{1-x}As$ were used for the active layer, then x = 0.2 could be used and the active layer thickness could be 50 Å. The quaternary solid solution $(Al_xGa_{1-x})_yIn_{1-y}P$ can lattice match GaAs[9] and have an energy gap in excess of 2.3 eV and provide the necessary carrier confinement. There are numerous other choices which

could be examined to determine which are the most reasonable heterostructures to grow. With the very active research in strained layer superlattices, results can be expected which would apply to this application.

IV. CONCLUSIONS

Electrical measurements were made on capacitors prepared with RPECVD SiO_2 films on p-type $Ga_{0.47}In_{0.53}As$ at low substrate temperatures. These measurements demonstrated that the RPECVD dielectric is suitable for use in the fabrication of MISFETs. Measurements on RPECVD SiO_2 layers on Si showed that care must be taken in cleaning and processing to prevent Na ions from being introduced into the dielectric layers. To provide stable characteristics, surface cleaning before deposition must be investigated and processing techniques must be used to prevent the introduction of mobile ions into the deposited dielectric layers. Techniques to reduce the temperature sensitivity of the threshold current density of InP-$Ga_xIn_{1-y}As_yP_{1-y}$ DH lasers were investigated. The most promising technique is the use of thin pseudomorphic active layers and wide energy gap cladding layers.

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We would like to thank R. J. Markunas of RTI for his cooperation and technical guidance during these studies.

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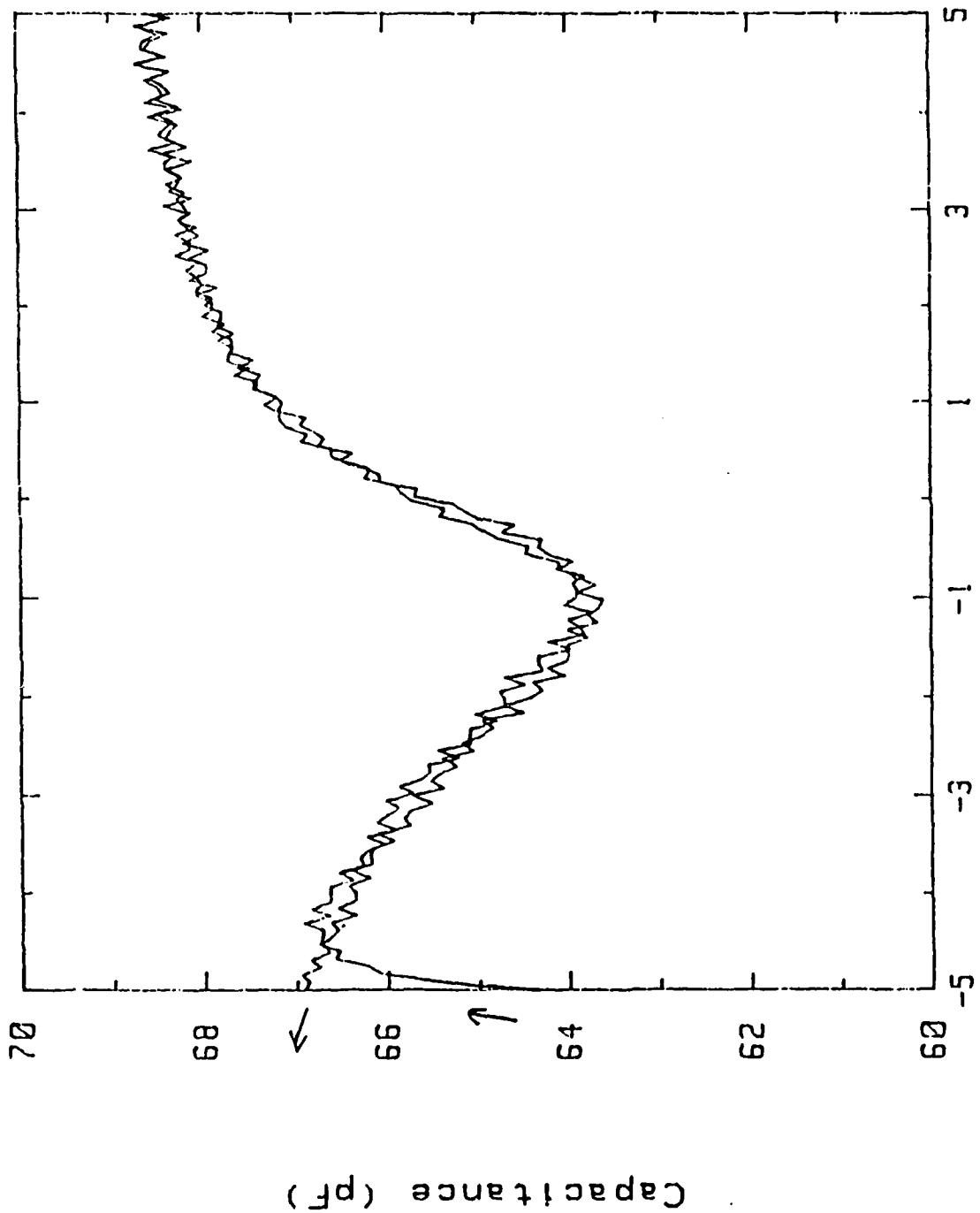

Fig. 1. Capacitance-voltage measurement of MIS capacitor at 500 Hz.

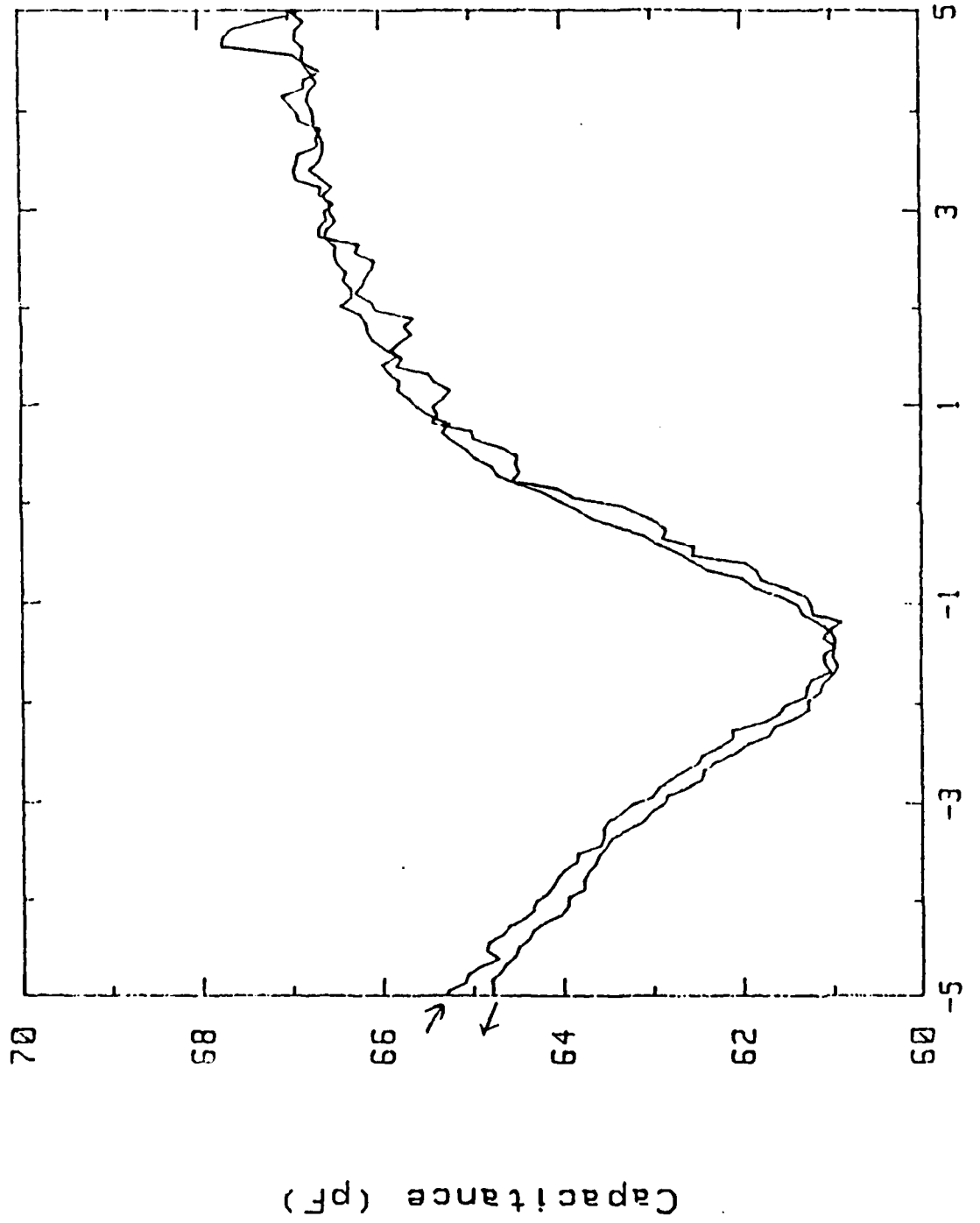

Fig. 2. Capacitance-voltage measurement of MIS capacitor at 5 kHz.

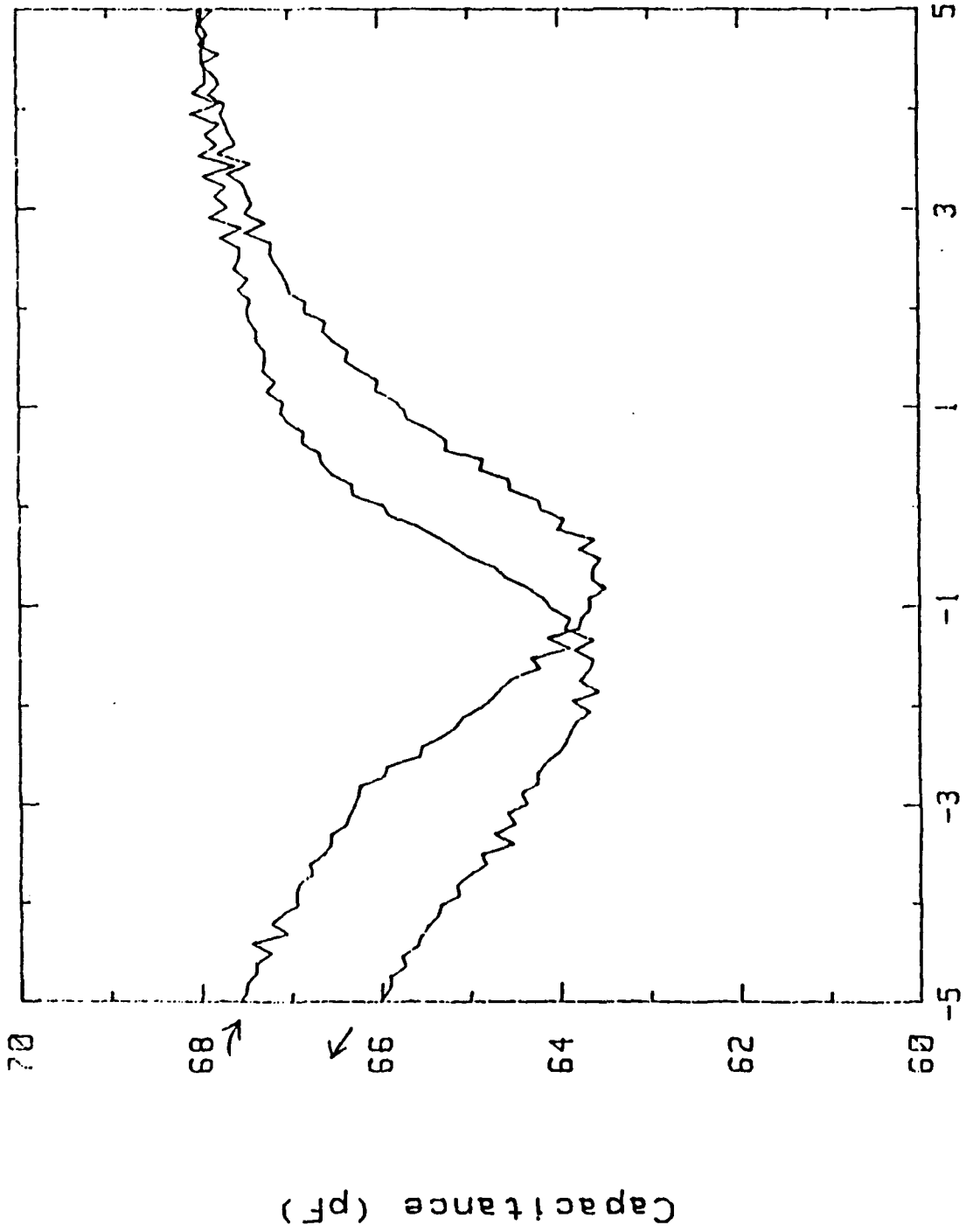

Fig. 3. Capacitance-voltage measurement of MIS capacitor at 1 kHz.

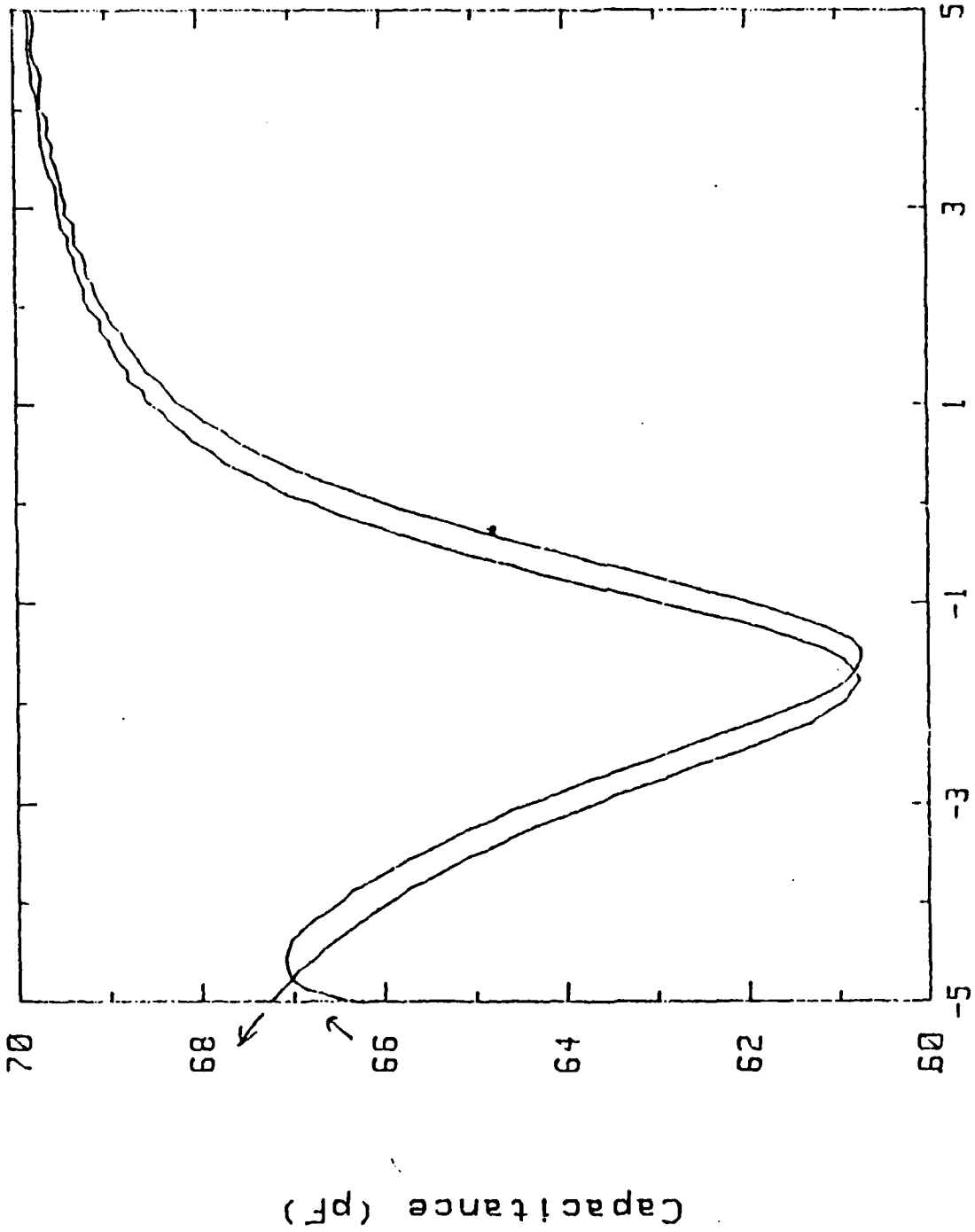

Fig. 4. Capacitance-voltage measurement of MIS capacitor at 10 kHz.

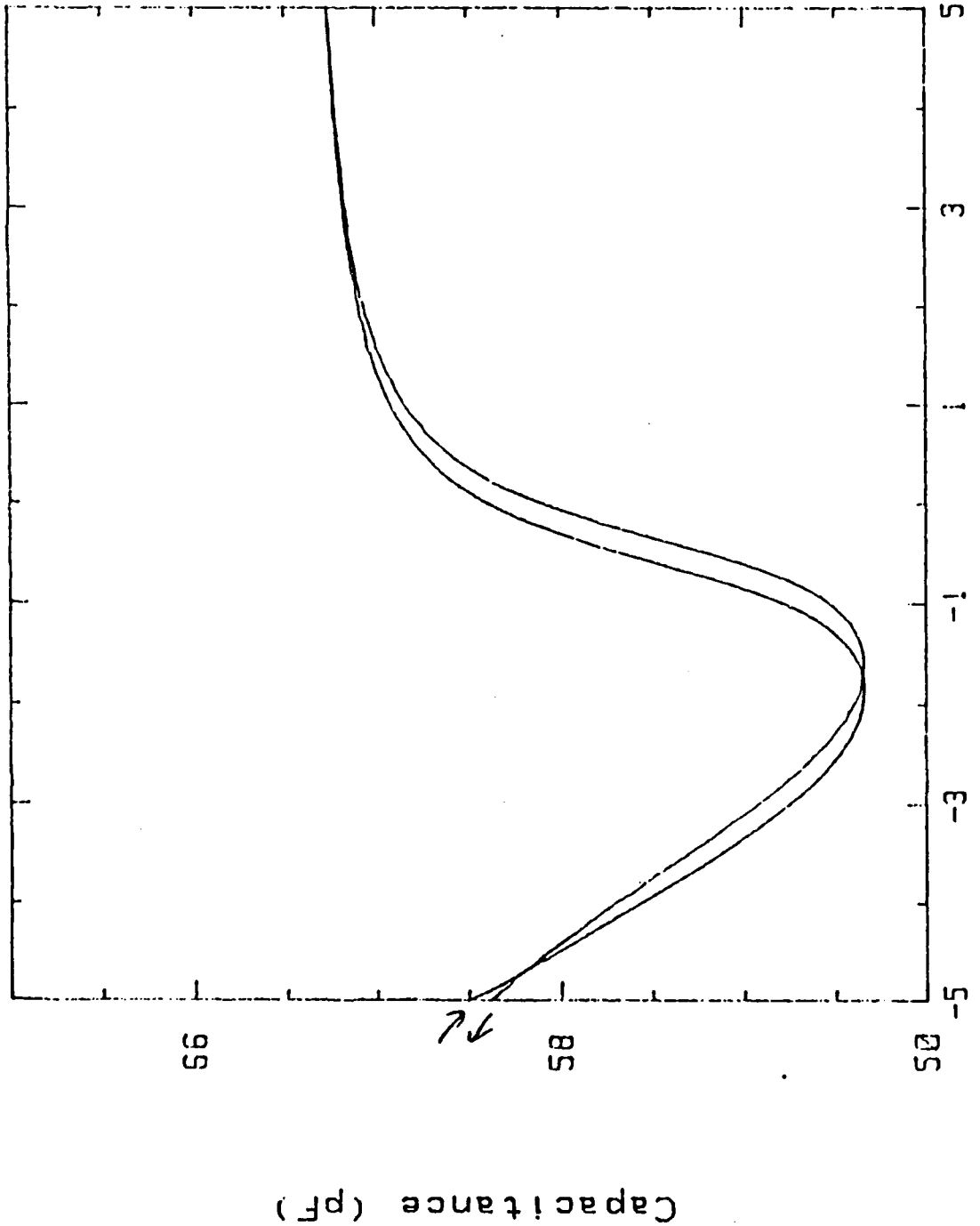

Fig. 5. Capacitance-voltage measurement of MIS capacitor at 50 kHz.

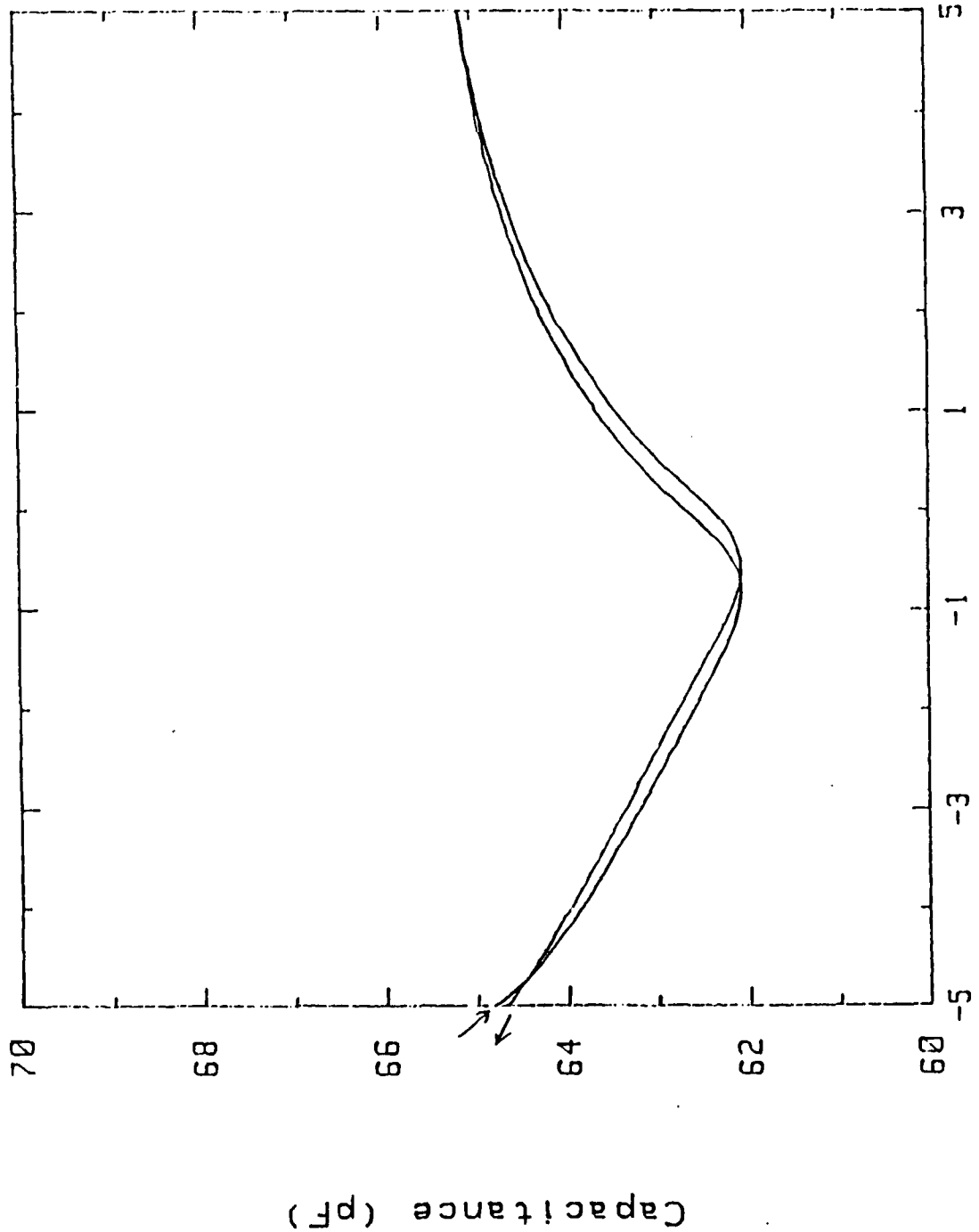

Fig. 6. Capacitance-voltage measurement of MIS capacitor at 1 MHz.

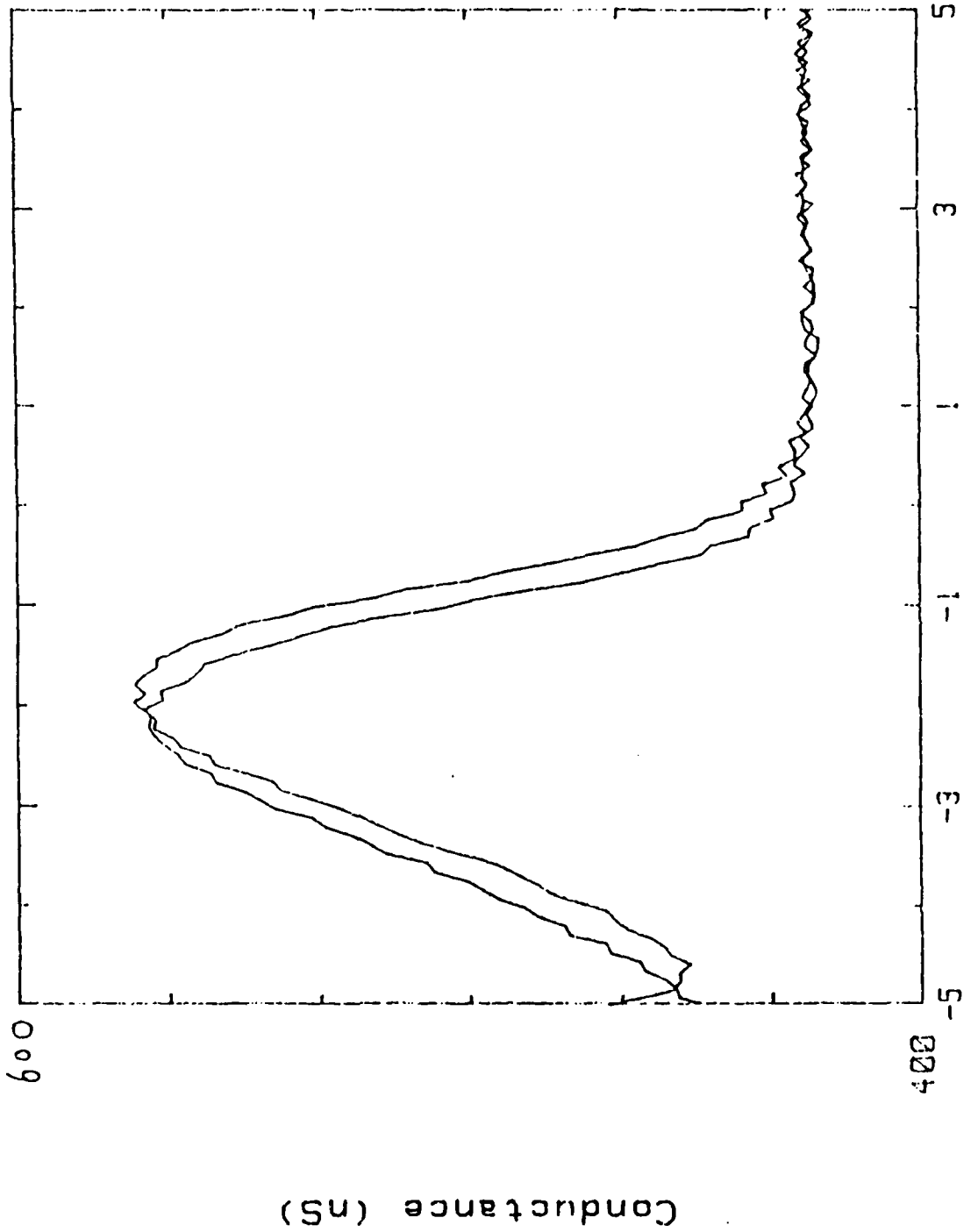

Fig. 7. Conductance-voltage measurement of MIS capacitor at 10 kHz.

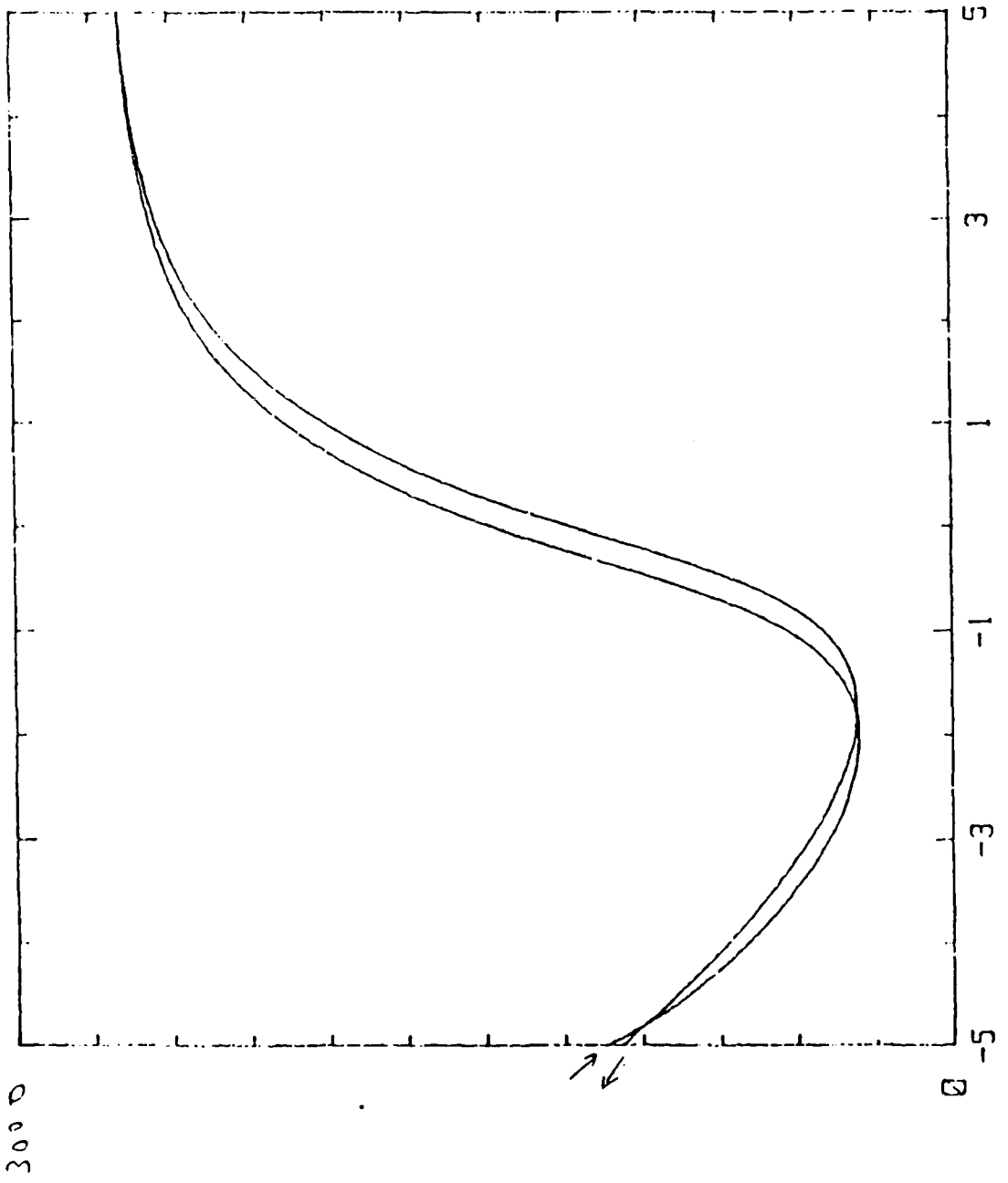

Fig. 8. Conductance-voltage measurement of MIS capacitor at 1 MHz.

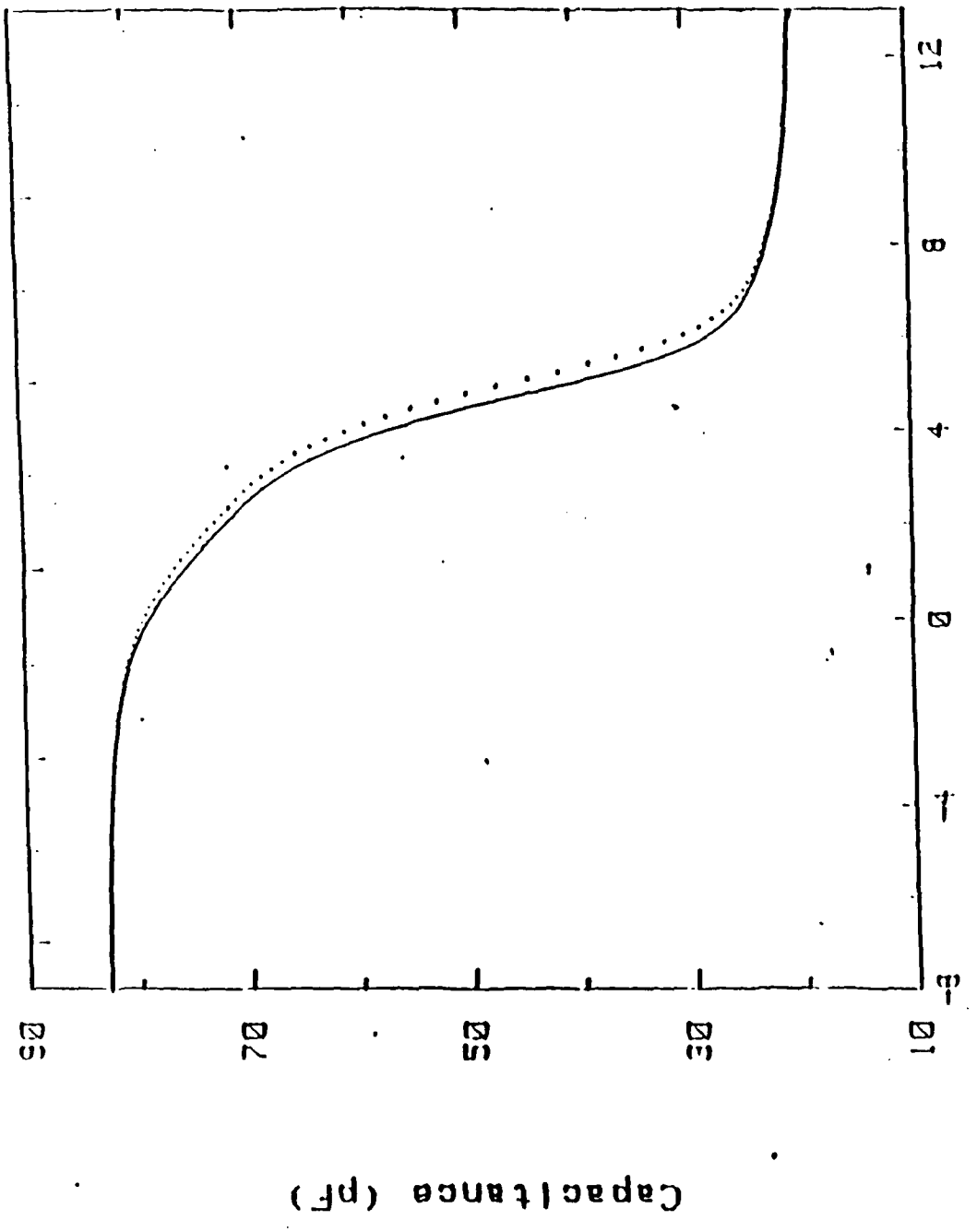

Fig. 9. 1 MHz C-V measurement

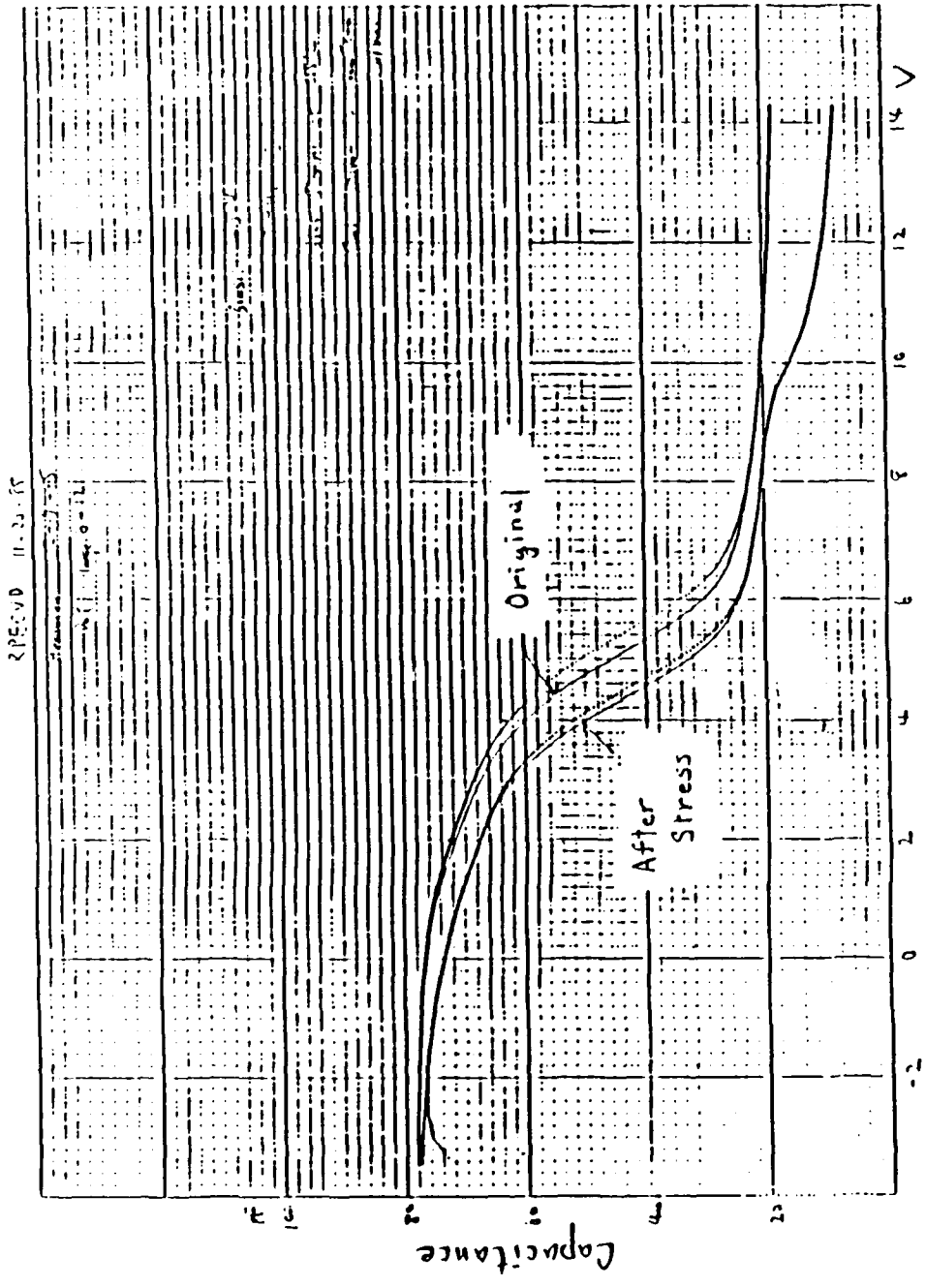

Fig. 10. Temperature stress bias measurement with +5 V bias

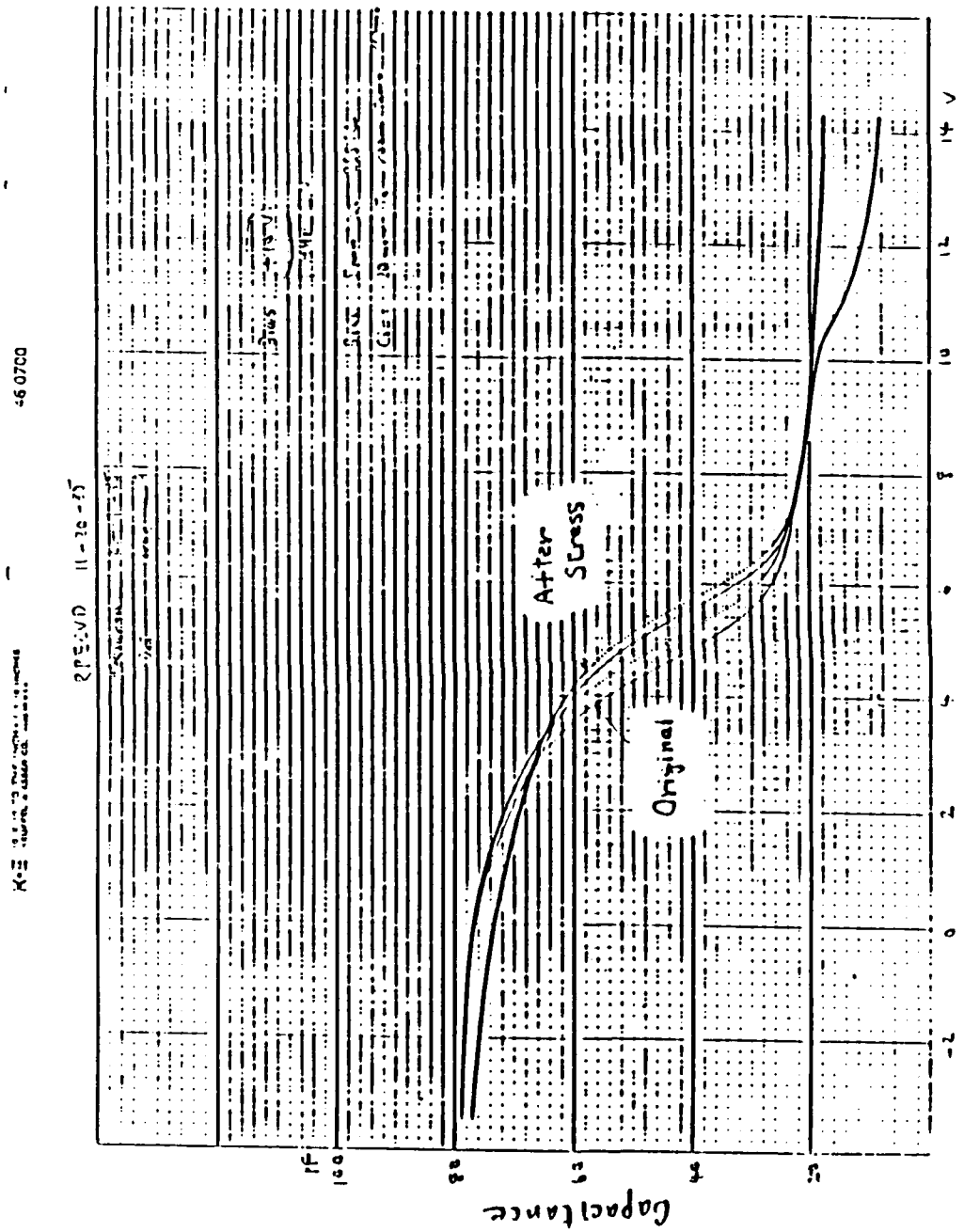

Fig. 11. Temperature stress bias measurement with +10 V bias

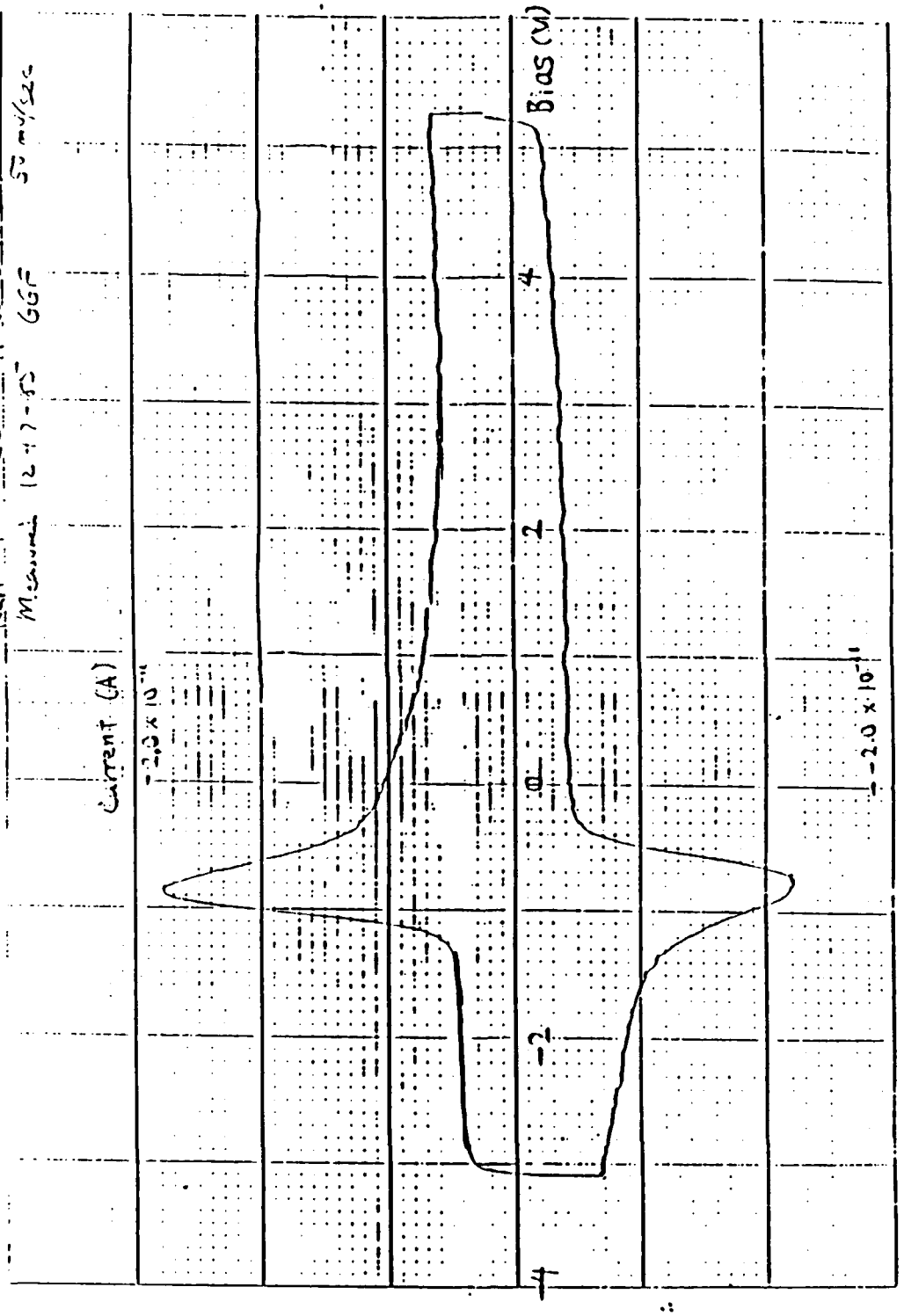

Fig. 12. Triangular voltage sweep measurement

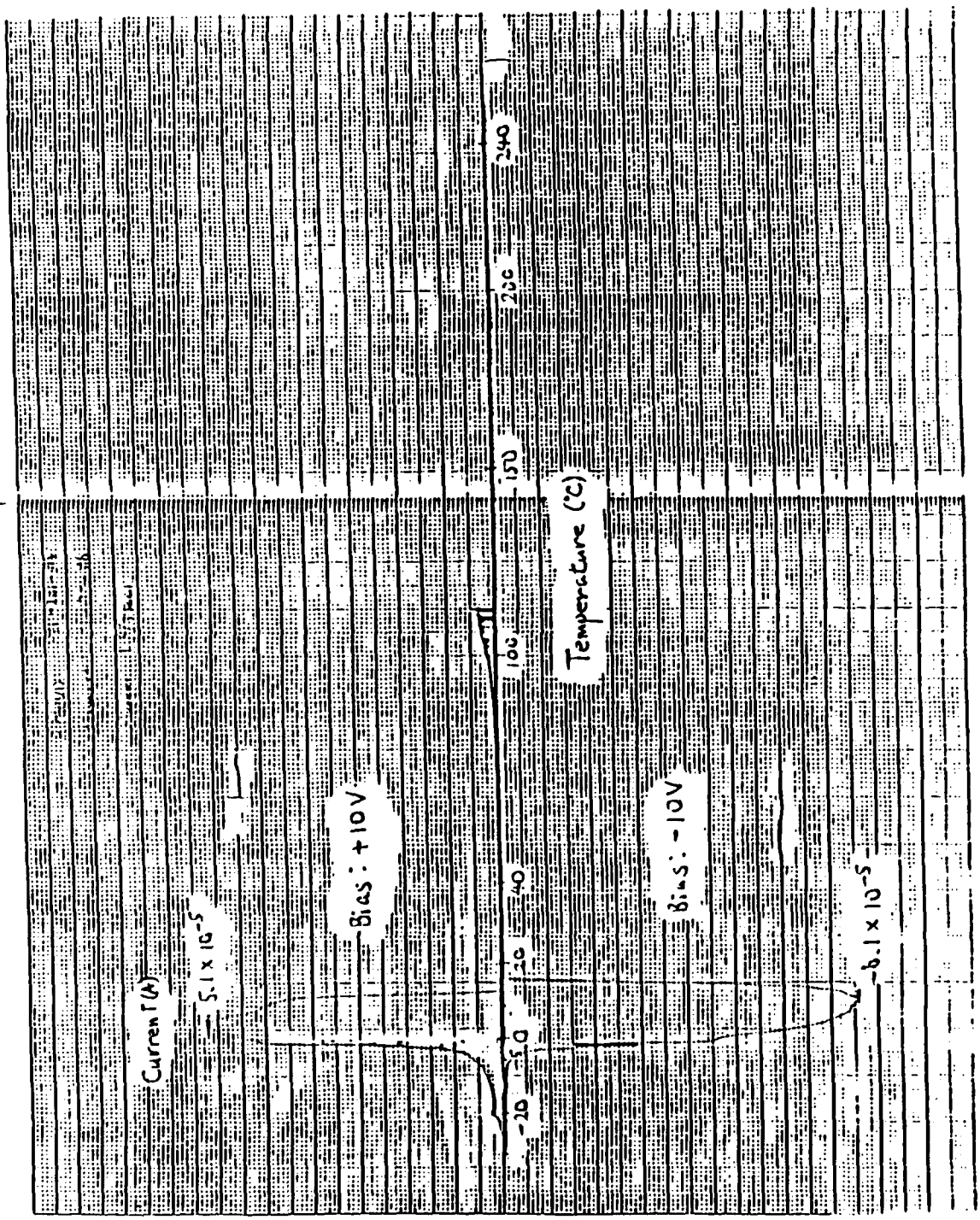

Fig. 13. Thermally stimulated ionic current measurement

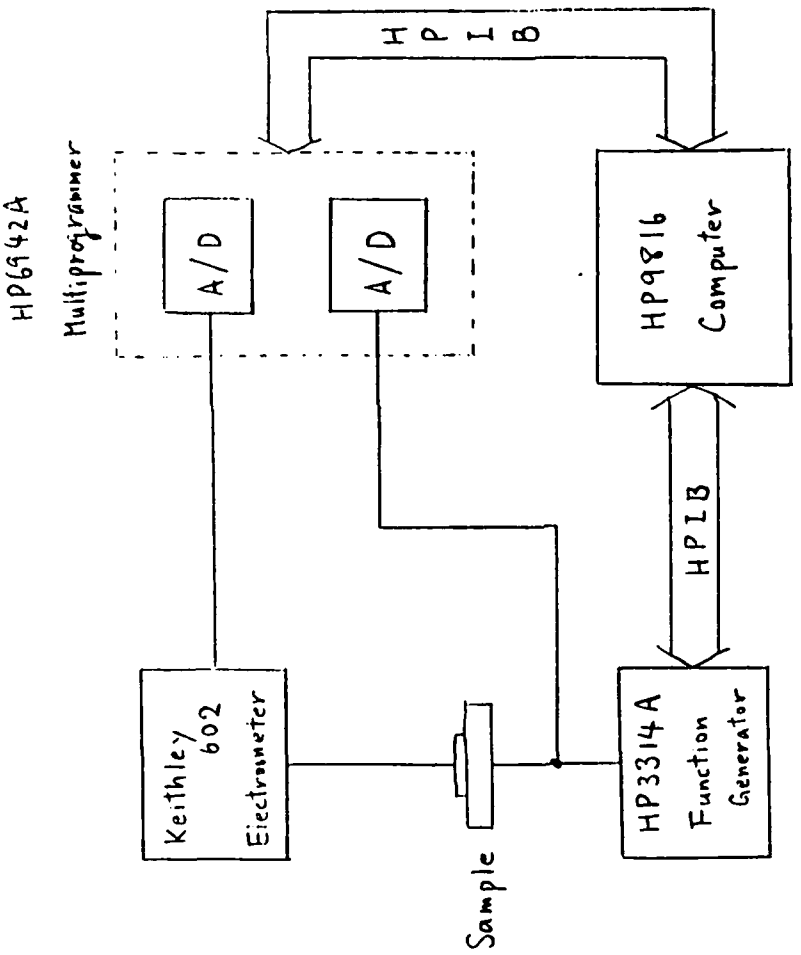

Fig. 14. Quasi-static and TVS measurement system.

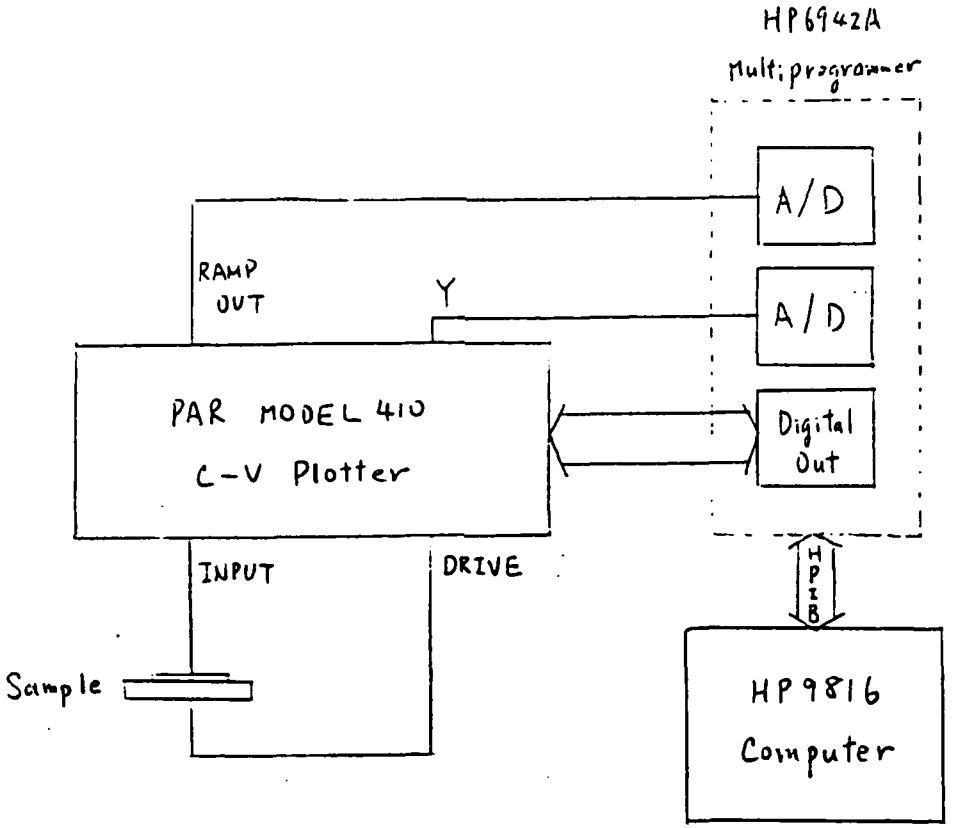

Fig. 15. High frequency C-V and G-V measurement system.

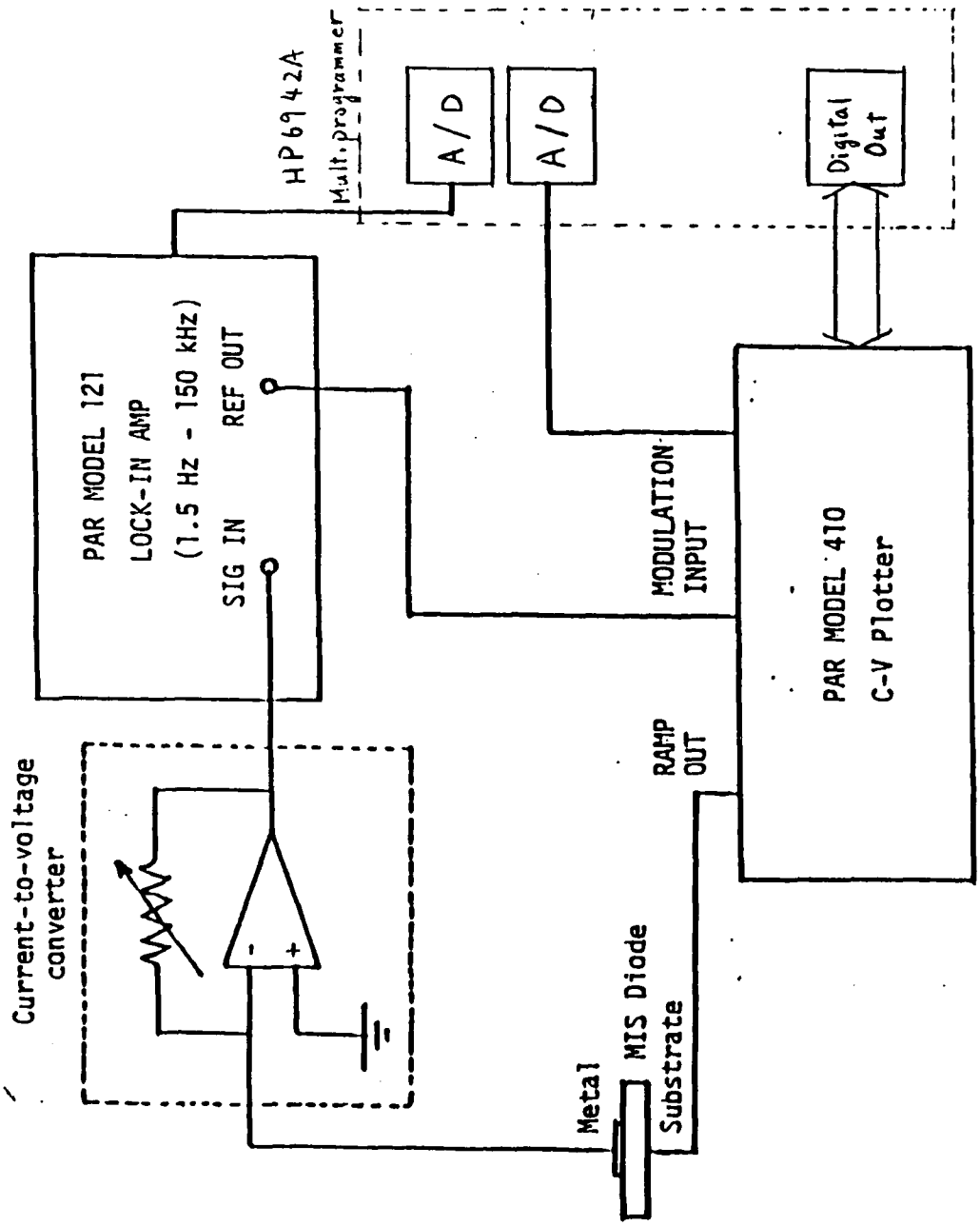

Fig. 16. Low and medium frequency C-V and G-V measurement system.

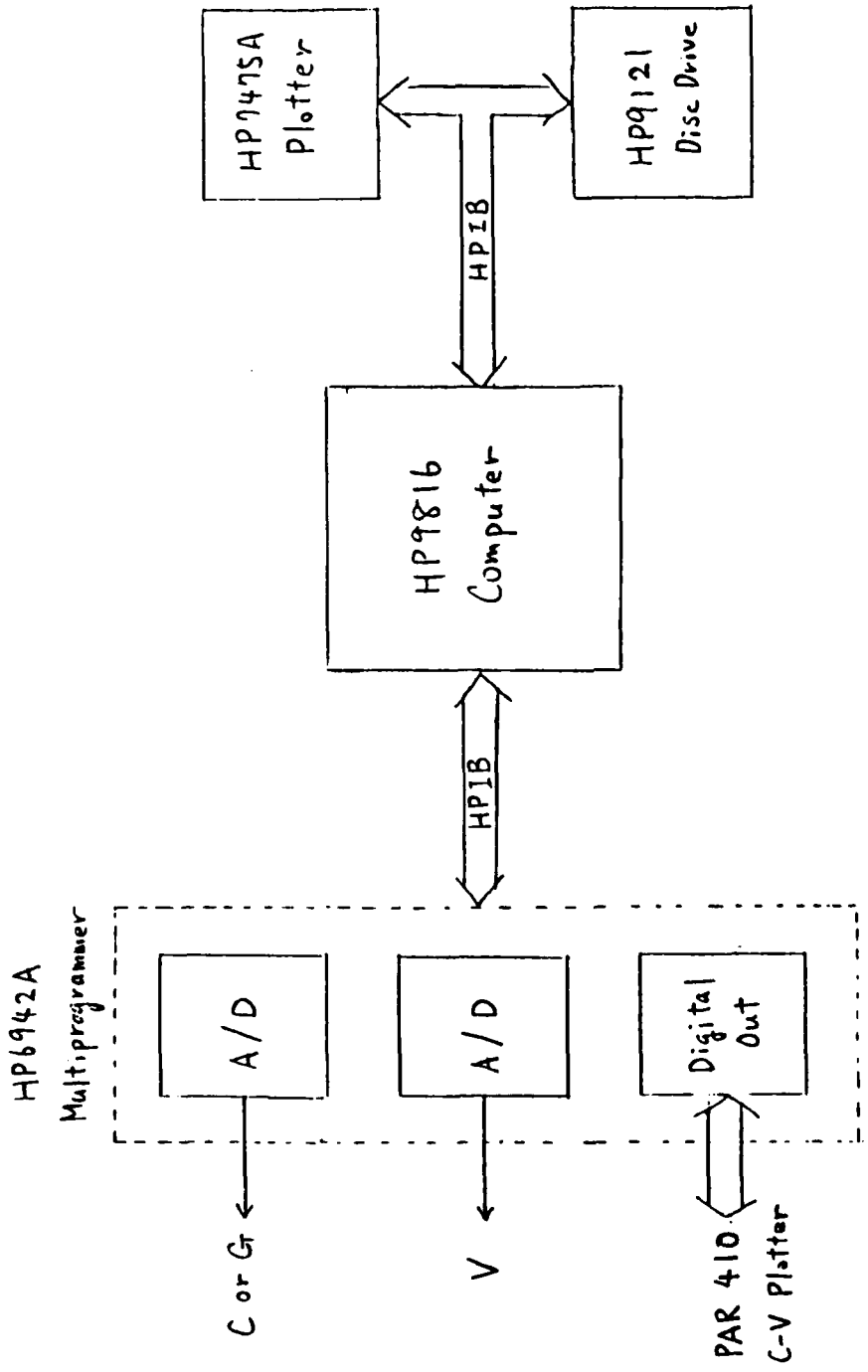

Fig. 17. Data acquisition and analysis system.

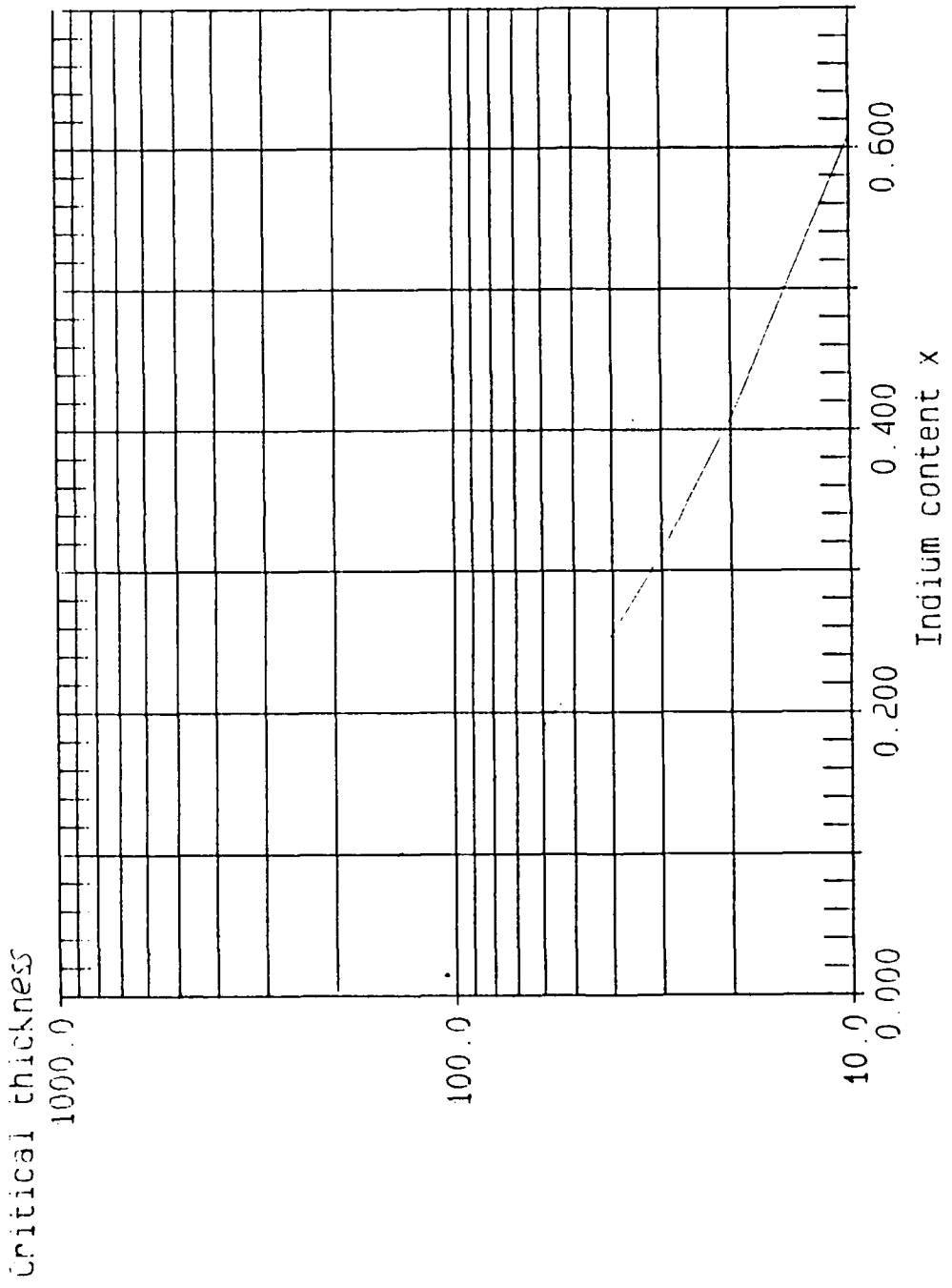

Fig. 18. Critical Thickness of a Ga_xIn_{1-x} Layer on GaAs.

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